

HPCN TTN



CAPRICE

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ESPRIT HPCN PST

DAPPER

**Distributed and Parallel Application of
PCB Placement Methods for
EMC Driven Design**

December 31, 1998

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Acronyms

ADVANCE	Advancing Common Basic Services for Distributed Concurrent Engineering Applications
B&B	Branch and Bound
BOSCH	Robert Bosch GmbH
CAD	Computer Aided Design
CAPRICE	Centre for Accessing HPCN Best Practice Information, Technology and Application Environments
CORBA	Common Object Request Broker Architecture
DAPPER	Distributed and Parallel Application of PCB Placement Methods for EMC Driven Design
DCAP	Decoupling Capacitor
DLR	Deutsche Forschungsanstalt für Luft und Raumfahrt e.V.
EC	European Community
ECU	European Currency Unit
EMC	Electromagnetic Compatibility
ESPRIT	European Commission Specific RTD Programme in the Field of Information Technology
FED	Fachverband Elektronik Design
GUI	Graphical User Interface
HPCN	High Performance Computing and Networking
IC	Integrated Circuit
ILP	Integer Linear Program
INCASES	INCASES Engineering GmbH
JESSI	Joint European Submicron Semiconductor Initiative
MCM	Multi Chip Module
MILP	Mixed Integer Linear Program
MPI	Message Passing Interface
PCB	Printed Circuit Board
PCC	Project Control Committee
PVM	Parallel Virtual Machine
PST	Preparatory, Support and Transfer
PTC	Project Technical Committee
SME	Small and Medium Sized Enterprises
TTN	Technology Transfer Node
WIDIS	Wissenschaftliche Dienstleistungen für Informatik und Systemtechnik GmbH

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Distributed and Parallel Application of PCB Placement Methods for EMC Driven Design

Abstract

Keywords:

PCB layout design, placement, EMC, parallel computing, high performance computing

Due to new technologies and EC regulations the importance of EMC problems for PCB layout design is growing significantly. For this reason, new layout tools for placement and routing are necessary to support the design process.

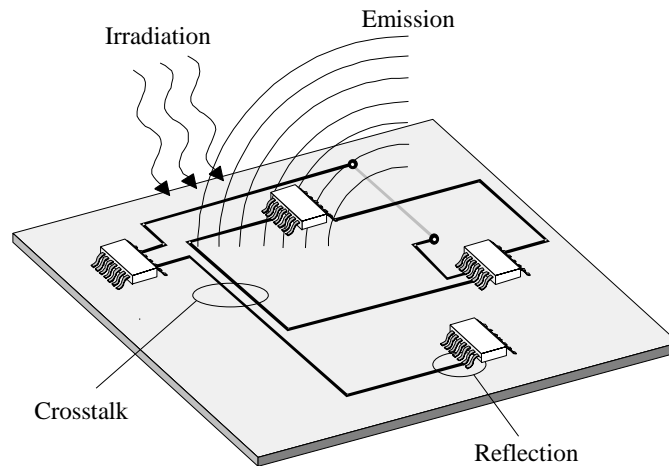
As a demonstration action project DAPPER (Distributed and Parallel Application of PCB Placement Methods for EMC Driven Design, ESPRIT 24448) has been set up to get a sequentially working EMC driven placement tool on the leading edge of the EC electronic market by using distributed computing.

Project Partners



1 Synopsis

Due to new technologies and EC regulations the importance of EMC (ElectroMagnetic Compatibility) problems for PCB (Printed Circuit Board) design is growing significantly. To cope with the problems EMC has to be considered during the development step in an early stage. For this reason, new layout tools for placement and routing are necessary to support the design process.



In the frame of project DAPPER (Distributed and Parallel Application of PCB Placement Methods for EMC Driven Design, ESPRIT 24448) the sequentially working placement tool PLACE-BOX for EMC driven PCB design was parallelised and the main algorithms and features were integrated into PCB design system THEDA. In order to obtain the scheduled time efficiency the placement tool is working on a cluster of workstations.

Depending on the design task the new placement tool based on HPCN technology is able to reduce the overall board design time up to 15 percent. By taking EMC requirements during placement into account the tool can reduce the number of design cycles and can avoid time consuming and expensive redesigns. This meets the strong demands of the end-users of decreasing the time to market for their designs. The consideration of EMC constraints in an early stage of the design process ensures a higher quality of the products. Based on distributed processing the tool with its time behaviour is well suited for interactive design work. Since the tool is working on a cluster of workstations no investment in specialised and expensive hardware is necessary. Therefore, the placement tool can be easily used in SMEs. The project outcome increases the competitiveness of the end users and will be delivered to market.

The project involved one technology provider: WIDIS, one HPCN expert: University of Paderborn and two end-users: BOSCH and INCASES. The project has been supervised by the CAPRICE TTN.

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2 Executive Summary

2.1 Overview

The task to design PCBs is becoming more and more complex. This is caused by new sub-micron designs, new packaging technologies, increasing number of connections that have to be considered, increasing processing speed of digital circuits and increasing share of mixed analog/digital circuits in microelectronic devices. Therefore electromagnetic noise effects have become major disturbing factors, causing loss in performance, logic errors or environmental pollution. The most important EMC problems on a PCB are reflections, crosstalk, radiation and irradiation. The magnitude of these electromagnetic disturbances are essentially influenced by the layout (placement, routing). In order to cope with the problems EMC has to be considered during the development step by appropriate design rules in an early stage. For this reason, new layout tools for placement and routing are necessary to support the design process.

WIDIS has developed a placement tool PLACE-BOX for EMC driven PCB design in the frame of project JESSI AC-5. This tool consists of a pool of several global optimising methods. The placement computation is based on cyclic application of these methods, which is very time consuming. In order to compete on the market PLACE-BOX had to perform much speedier as it did.

DAPPER demonstration project objective was to demonstrate the economical benefit of the application of HPCN technologies in the field of PCB layout design. The two main tasks of the project were the parallelisation of placement tool PLACE-BOX and the integration into PCB design system THEDA.

2.2 Approach

The only way for a significant computation time reduction of placement tool PLACE-BOX was to break up the cyclic application of the methods by using parallel, distributed processing on a cluster of workstations. The project partners developed a concept for distribution and integration. After evaluation of different systems PVM was defined as the platform to distribute the computations. For the parallel PLACE-BOX we use a combination of a master-slave and tree process model. The master process contains the control unit of PLACE-BOX, which is responsible for process spawning, initialisation and collection of the results. The slave programs perform the actual placement computation. The tree computation model was applied to implement the parallel MILP solver efficiently. The control unit is integrated into two alternative master processes. One is the graphical user interface (GUI) based on TCL/TK and the other is the design system THEDA.

2.3 Major Achievements

The parallel placement tool is realised as proposed. It was successfully applied to different demonstration examples and during the evaluation phase to latest designs of the end-users. These boards were manually placed and routed in the companies. The design processes were very time consuming due to the extreme board complexity and many restrictions. Based on the

gathered results it was shown that the parallel tool can reduce the computation time for placement significantly. Depending on the design task the new placement tool can decrease the overall design time up to 15 percent. Based on the technological progress the project was faced with demands by the end-users for new placement features. Therefore, several new methods are developed and integrated in PLACE-BOX, e.g., a new sophisticated method for placing decoupling capacitors. The placement tool is successfully integrated into the PCB design system THEDA. This integration is a prerequisite for evaluation and for usage in the design departments of the end-users.

2.4 Expected Benefits

- **Decreased time to market**

Depending on the design task the total design time can be reduced up to 15 percent by using the HPCN based tool.

- **Reduced prototyping**

By taking EMC requirements during placement into account the tool can decrease the number of design cycles and can avoid time consuming and expensive redesigns.

- **Higher product quality**

The consideration of EMC constraints in an early stage of the design process ensures a higher quality of the products.

- **Improved design work**

Based on distributed processing the tool with its time behaviour is well suited for interactive design work.

- **Usage in SMEs**

Since the tool is working on a cluster of workstations no investment in specialised and expensive hardware is necessary. Therefore, the placement tool can be easily used in SMEs.

- **Increased competitiveness**

The project outcome increases the competitiveness of the end-users and will be delivered to market.

3 Full Technical Text

3.1 State of the Art

3.1.1 Introduction to the Project

DAPPER demonstration project objective is to demonstrate the economical benefit of the application of HPCN technologies in the field of PCB layout design.

Due to new technologies and EC regulations the importance of EMC problems for PCB design is growing significantly. For this reason, new layout tools for placement and routing are necessary to support the design process. At present, there is no automatic placement tool for PCB design on the market capable of considering highly complex EMC design rules.

In the frame of project JESSI AC-5 placement tool PLACE-BOX was developed for EMC driven PCB design by WIDIS. This tool consists of a pool of several global optimising methods.

The main problem with using efficient global optimising methods are the numerous thermal, EMC, manufacturability and other geometrical constraints that have to be considered simultaneously. Advanced PCB placement methods have to take into account the following rules e.g.:

- High-speed constraints given by net rules.
- Definition of component groups to place such group in coherent area.
- Admissible and prohibited placement areas.
- Floor-planning concept.
- Minimum and maximum distances between component pairs.
- Arbitrarily shaped placement areas.
- Preplaced components.
- Stacked subboards.

In PLACE-BOX the problem of handling the constraints simultaneously is solved by decomposing the problem in the two phases global placement and final placement. For both phases one or a combination out of several methods can be applied (Figure 1).

In the first phase a component placement is computed, which still may contain violations of geometrical constraints, such as component overlaps, minimal distances for neighboured components due to manufacturability requirements or a placement of components inside keepouts or outside of the placement area. For this phase the partitioning and quadratic optimisation method is mainly used in PLACE-BOX.

The second phase offers methods to resolve miscellaneous geometrical constraint violations, to spread or to align components. Another possibility is to place a restricted number of components in a sub-region (e.g. supplied by partitioning) by formulating the problem as a mixed integer linear program (MILP). These sub-problems are solved by a dedicated MILP-solver.

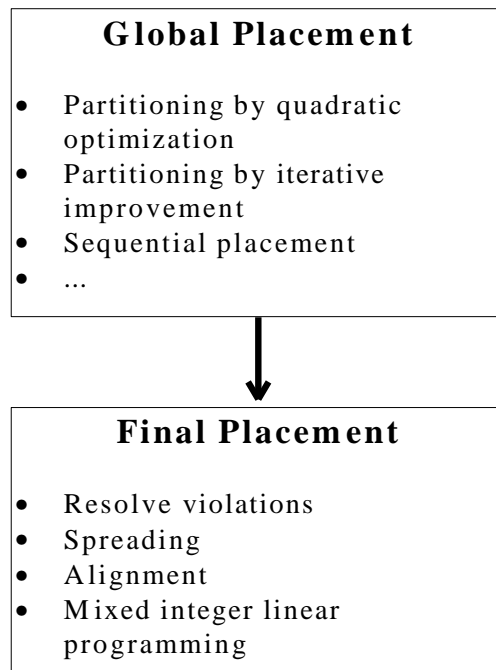


Figure 1: The two phases of PLACE-BOX

PLACE-BOX consists of a pool of several global optimising methods. Each of these methods is controlled by different parameters. The computation of a near-optimal PCB placement assumes an appropriate choice of these parameters. Since an analytical calculation of optimal parameter values is impossible, PLACE-BOX computes a good placement by cyclic application of these methods with different parameter values. This is a time consuming procedure.

In order to compete on the market PLACE-BOX had to perform much speedier as it did. The way for a significant computation time reduction was to break up the cyclic application of the methods by using parallel, distributed processing on a cluster of workstations.

Company WIDIS is the technology provider in the DAPPER project. The University of Paderborn provided the required parallelisation and distribution know-how. The end-users BOSCH and INCASES have a strong interest to use the advanced placement tool in their own PCB design and service departments. The knowledge of these departments was provided by both companies in the project.

The partners intend to exploit the result of the project in order to increase their competitiveness. The product will be sold as an add-on option to the THEDA product line.

3.1.2 Project and Business Objectives

- Parallelisation of placement tool PLACE-BOX by distributed processing to reduce the computation time significantly.
- Providing a tool which supports the efficient design of PCBs using HPCN technology.
- Increase the productivity of PCB designers to allow demands of decreasing time to market targets to be met.

- Integration of the placement tool into PCB design system THEDA.
- Taking EMC constraints in an early stage of the design process into account to ensure higher quality of the products and to reduce the number of design cycles.
- Increasing the competitiveness of the end-users by using the tool.
- Maintaining the usability of the tool in SMEs by using workstations as hardware platform.
- Supporting the transfer and distribution of HPCN technologies in electronic companies.

3.2 Approach

3.2.1 System for Distributed Computing

After project start WIDIS and University of Paderborn compared and evaluated PVM (Parallel Virtual Machine), MPI (Message Passing Interface), the services provided by the ESPRIT project ADVANCE and CORBA (Common Object Request Broker Architecture) for their usage in the DAPPER project. Criteria for the evaluation were the effort to implement the desired communication over a cluster of workstations, the supported operating systems, the availability of the software and the effort to implement fault tolerance concerning hosts or tasks failures.

Under this criteria PVM was chosen. MPI is designed for a high performance on massively parallel processors and has no or poor features on interoperability between different architectures. In CORBA the effort to implement the simple form of communication required in the parallel PLACE-BOX is higher by far. PVMs powerful set of dynamic resource manager and process control functions and the stability and availability of the software on all platforms makes it favourable over the ADVANCE-services.

3.2.2 Activities for Parallelisation and Distribution

WIDIS and University of Paderborn analysed and evaluated PLACE-BOX methods and algorithms suited for parallelisation and distribution. As a result the following main activities were done in the DAPPER project to realise the envisaged parallel PLACE-BOX:

- A control unit able to analyse the placement task and to define appropriate methods of the PLACE-BOX to solve the problems had to be implemented. This control unit should be part of two alternative master processes: The 'lean' master should provide in addition to the control unit a graphical user interface (GUI) for parameter selection and visualisation of the results. The other master process in which the control unit should be integrated is THEDA, where the parameter selection and the visualisation of the results is done according to the look & feel of the THEDA user interface. An application program (slave) with all placement methods had to be implemented and should run over the workstation network. For the placement computation the control unit distributes the work in the network and evaluates the results.
- The cyclic application of the partitioning and quadratic optimisation method with different parameters had to be broken up. A procedure had to be implemented to supply the control unit with appropriate different parameter sets. According to the number of parameter sets

the control unit distributes a modified version of the partitioning and quadratic optimisation method in the network supplied with these parameter sets.

- Based on a prototype of a parallel MILP-solver available at the University of Paderborn, a dedicated MILP-solver which exploits the special structure of placement problems had to be developed. The MILP-solver uses a Branch and Bound technique. This technique is able to find the optimal solution for the given objective function. But depending on the number of integer variables, which increases with the number of considered components, the run time increases dramatically. Therefore we use a parallel MILP-solver, which distributes the work on a cluster of workstations using PVM.

3.2.3 Description of the Parallel PLACE-BOX Version

For the parallel PLACE-BOX version we used a combination of master-slave and tree computation model (Figure 2). The master process contains the control unit of PLACE-BOX, which is responsible for process spawning, initialisation and collection of the results. The slave programs perform the actual placement computation. The tree computation model is applied to implement the parallel MILP solver efficiently.

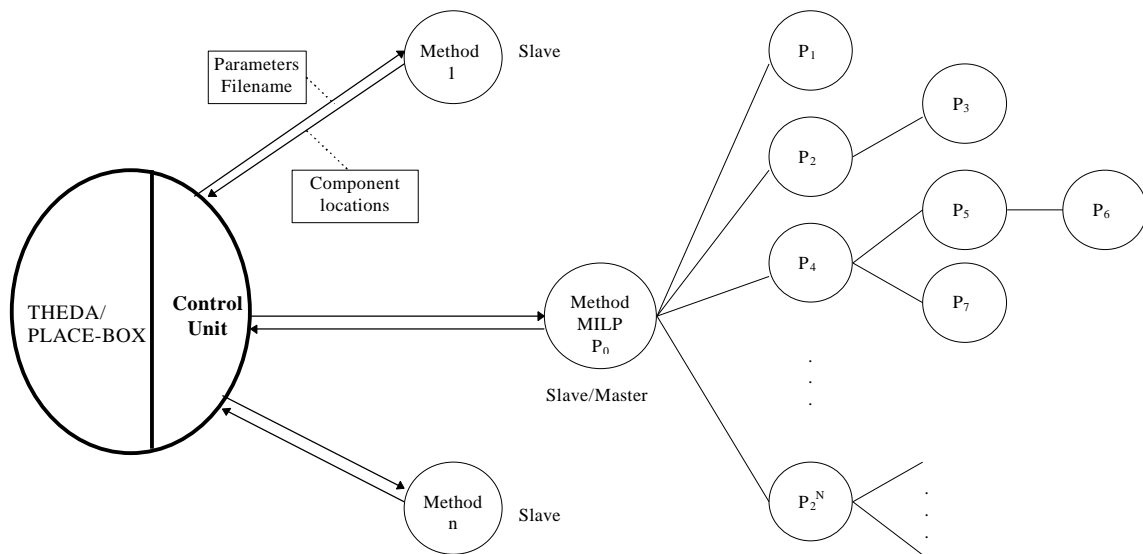


Figure 2: The combined master-slave and tree computation model of PLACE-BOX

3.2.3.1 *The Master-Slave Computation Model in PLACE-BOX*

The control unit should be integrated into two alternative master processes. One is the graphical user interface based on TCL/TK and the other is the design system THEDA.

The control unit has the following tasks in both systems:

- Analyse the placement task
- Selection of **n** appropriate solution methods
- Computation of parameter set
- Spawning of **n** copies of the application program (slave)
- Sending **file name** and parameters to the slaves
- Waiting for placement results
- Receiving placement results
- Evaluation of the results
- Killing the slave processes

The other parts of the master process have to provide the graphical user interface for the parameters and have to visualise the results after placement.

The application program (slave) with all placement methods has the following tasks:

- Receiving the **file name** of the placement task and the parameters from the master
- Reading the placement task from the **file**
- Compute the placement by application of method i ($1 \leq i \leq n$) with corresponding parameter set
- Sending the resulting component locations to the master.

Notes:

1. From the performance point of view it is a great advantage to send the file name of the placement task to each slave. The read process of a placement task takes only a couple of seconds (1-5 seconds). So, after reading the placement task each slave has stored all information of the task in the internal database. This means there is no communication among the slaves needed and large granularity is ensured.
2. Contrary to the sequential PLACE-BOX a new strategy of the partitioning and quadratic optimisation method had to be implemented. In order to break up the **m** times cyclic application of this method with different parameters the master spawns **m** slaves to compute solutions with this procedure in parallel.

3.2.3.2 *The Tree Computation Model in PLACE-BOX*

The tree computation model is applied to implement the dedicated parallel MILP solver efficiently.

Several optimisation problems can be formulated as Integer Linear Programming (ILP) problems of the form:

$$\min\{cx: Ax \leq b, x \in Z_+^n\}$$

and when relaxing the integrality constraint on some of the variables, we obtain Mixed Integer Linear Programming problems (MILPs). In PLACE-BOX placement sub-problems can be described as MILPs. In order to solve such a MILP efficiently a dedicated solver is necessary.

Most of the known solvers perform some pre-processing in order to improve ILP and MILP formulations of the problem. In our case pre-processing involves:

- searching for implicit bounds in the matrix,
- reduction of variables,
- removing of empty rows and columns, scaling rows and variables.

The MILP solver distributes task dynamically among the processors in order to improve the work load of processors and to minimise the communication .

The solver first uses a technique to reduce the number of variables, then Revised Simplex is used to solve the relaxed linear program (LP). From this a B&B algorithm is employed to solve the MILP. The B&B-tree is traversed in depth-first order because this minimises the memory requirements. The algorithms used in the solver are developed for MILP problems with sparse constraint matrices (0.1%-10% non-zero elements).

3.2.4 *The Graphical User Interface*

To improve the interactive design process and to use the placement methods and features efficiently a new graphical user interface of PLACE-BOX had to be developed. This new GUI of PLACE-BOX was built on TCL/TK and is used to select and load placement tasks, to choose placement methods and parameters, to control the computation and to visualise and analyse placement results.

3.2.5 *Integrating PLACE-BOX into THEDA*

To integrate the PLACE-BOX into the THEDA design system the creation of the PLACE-BOX data-structure should be possible by reading a TL-file or a PBD-file. For the integration, the input of the placement problem has to be extracted from the THEDA-database. This database contains very detailed geometrical information about the layout. The crucial task of realising an interface is to find an appropriate level of abstraction for these details such that the information provided are detailed enough to avoid violations of clearance rules and to be able to determine dense placement using tiny free spaces and on the other hand not to slow down the algorithms by considering unnecessary details. Moreover THEDA had to be extended to

supply dialogue windows for the placement parameters and to select placement methods. These parameters had to be passed to PLACE-BOX as well. After the computation of PLACE-BOX has finished, the resulting component locations have to be transferred into the THEDA database and the result of the placement has to be displayed by the graphical user interface of THEDA.

3.3 Results, Achievements and Benefits

Both main tasks of the project the parallelisation of placement tool PLACE-BOX by using distributed processing and the integration into design system THEDA are realised as proposed.

3.3.1 Test Results

In this chapter we will describe the results of a demonstration of the code on a large example. The demonstration was carried out using hardware of the University of Paderborn. The placement methods used for computation are controlled by different parameters. The computation of a near-optimal PCB placement assumes an appropriate choice of the parameters. Since an analytical calculation of optimal parameter values is impossible the former sequential PLACE-BOX computes a good placement by cyclic application (8 times) of these methods with different parameter values. Therefore, the implemented control unit of the parallel PLACE-BOX is able to spawn 8 slave processes on the cluster of workstations. Each process performs the placement computation using its own parameter set.

3.3.1.1 Description of the Test Board

The used test board **s2** consists of 707 components and 765 nets. 18 components are preplaced. The placement task is to place the remaining 689 unplaced components on both sides of the board under rotation angles that are multiples of 90 degree unless placement rules for individual components fix their placement side or restrict their admissible rotation angles. In order to avoid EMC problems several net length restrictions are defined.

The sequentially working PLACE-BOX needs for the computation of the 8 cycles about 51 minutes to compute the placement result for this board.

The workstation cluster used for demonstration consists of 8 SUN Ultra 1 machines. Since the machines are part of the overall network of the University of Paderborn the load of the machines was not constant during the demonstration test.

The following Figure 3 shows the placement result computed by PLACE-BOX.

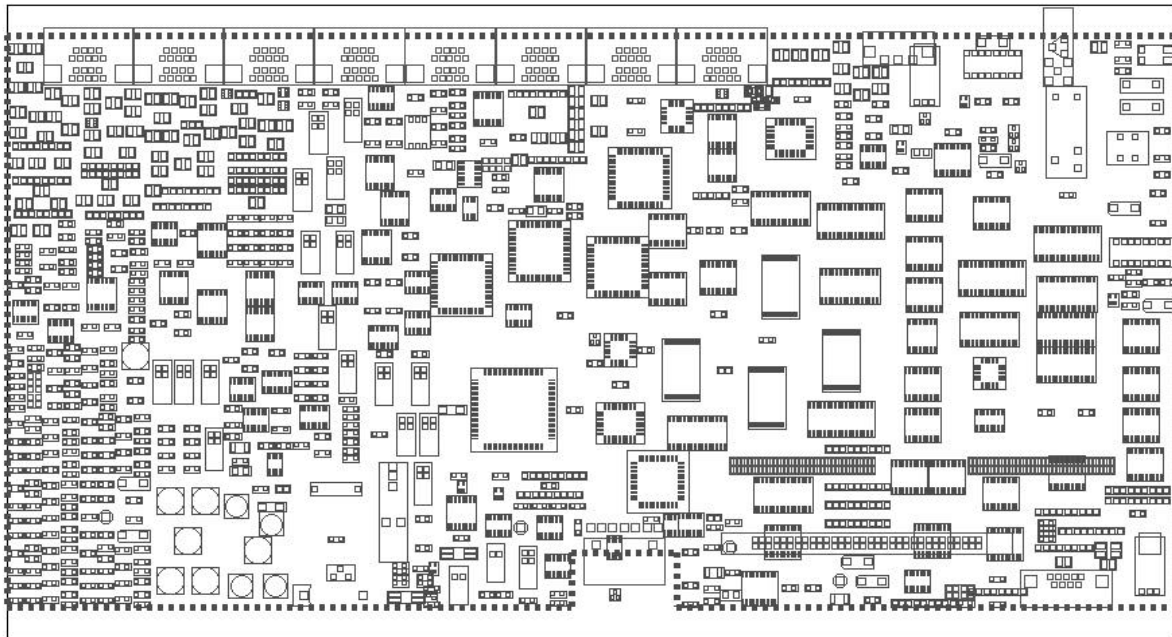
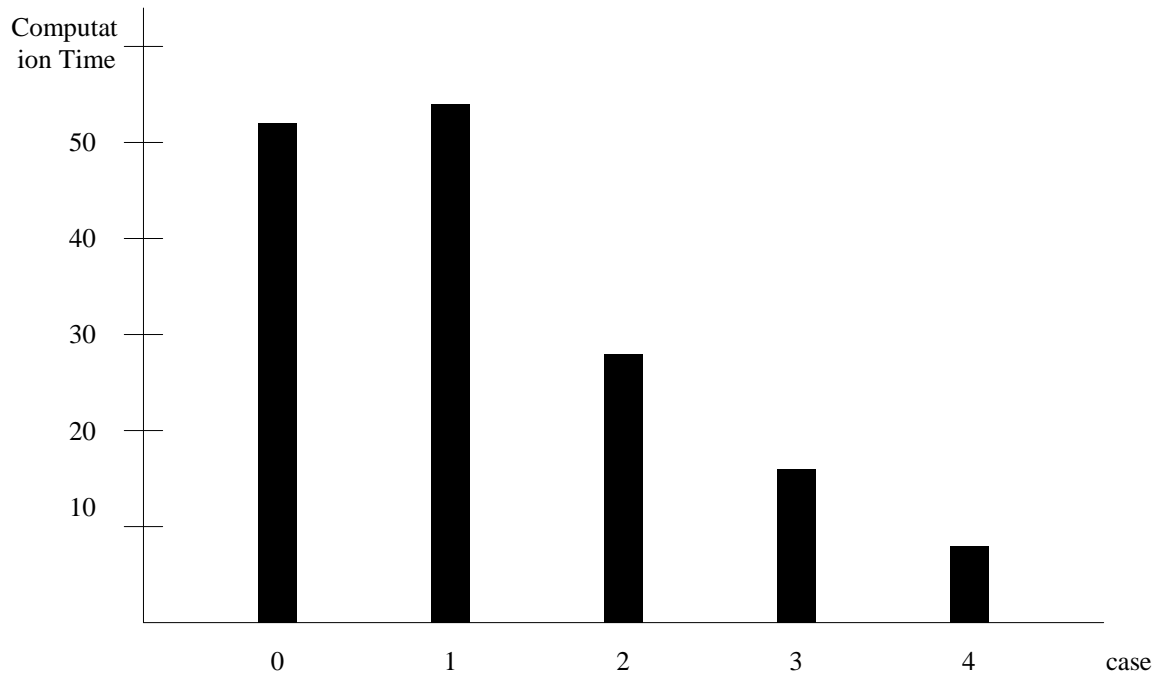


Figure 3: Placement result of board s2 computed by the parallel PLACE-BOX

As mentioned above the sequential PLACE-BOX (case 0) takes about 51 minutes to compute the placement result. For testing the parallel tool distributes the placement tasks in clusters of workstations of different sizes. The four used clusters of workstations consist of 1, 2, 4 and 8 hosts respectively. The needed computation time for the 4 cases is shown in the following table:

Case	Number of Hosts	Computation Time [Min]
1	1	54
2	2	28
3	4	15
4	8	8

The next figure gives an impression of the needed computation time in the 5 cases.



In comparison with the sequential PLACE-BOX (case 0) the computation time was

- case 1: increased by 5 percents
- case 2: decreased by 26 percents
- case 3: decreased by 70 percents
- case 4: decreased by 85 percents.

In case one the 8 spawned slave processes are running on one host. In comparison with the sequential PLACE-BOX there is an increase in needed computation time. This is caused by the higher communication effort between the master and the 8 slaves.

In the project programme it was scheduled to reduce the computation time for placing highly complex boards under 10 minutes. Based on the achieved results for this board this project objective is fulfilled. With this time behaviour the tool is well suited for interactive design work. The achieved speed by distributed processing is a strong prerequisite for the acceptance of the tool by layout designers.

3.3.2 Graphical User Interface

To improve the interactive design process and to use the placement methods and features efficiently a graphical user interface of PLACE-BOX was developed and built on TCL/TK. The interface is used

- to select and load placement tasks,
- to assign placement tasks to hosts of the PVM,
- to choose placement methods and parameters,
- to control the computation and
- to visualise and analyse placement results.

Figure 4 shows a snapshot of the GUI with different sheets. In the top sheet you can assign a placement method to a preferred host.

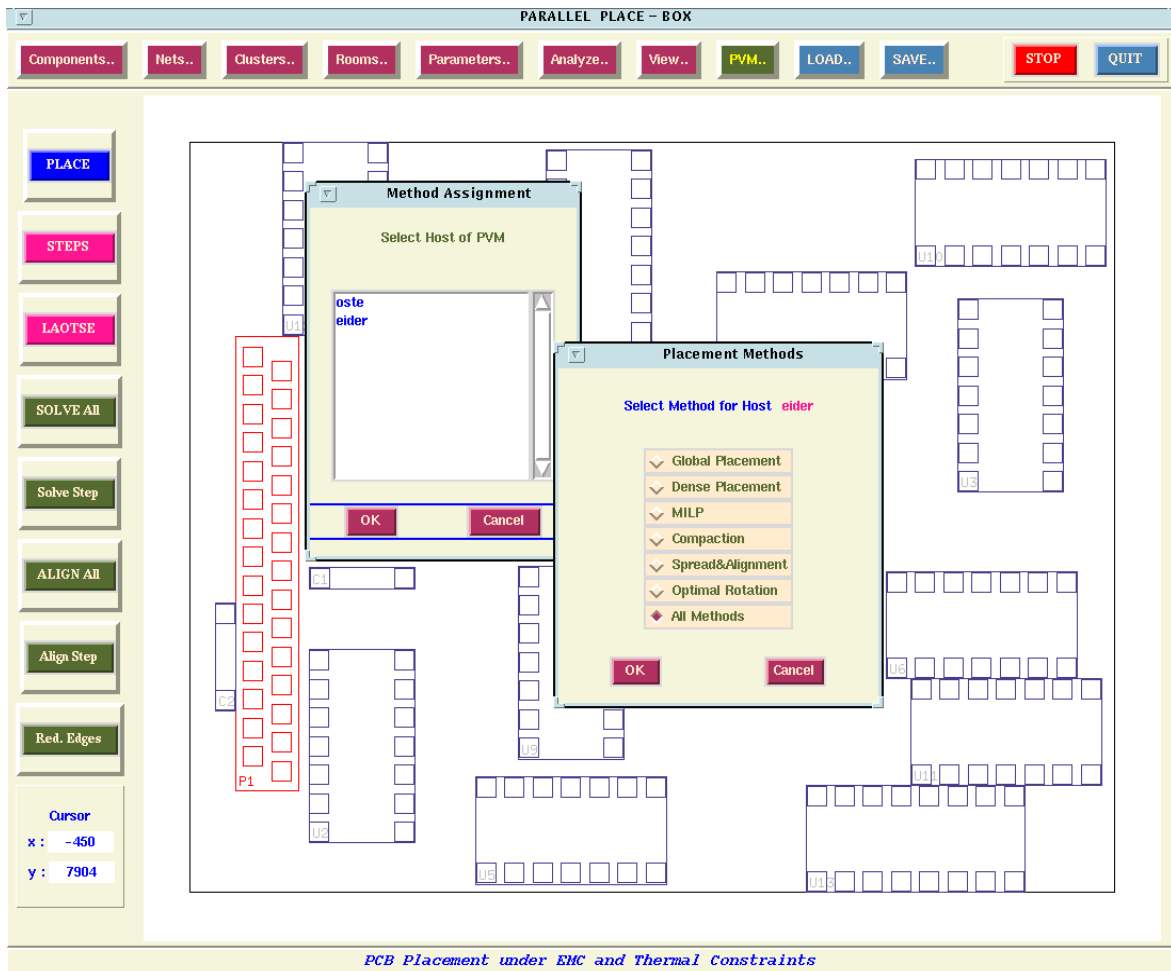


Figure 4: GUI of PLACE-BOX

Figure 5 shows how the very important aspect of electrical length violations can be watched in PLACE-BOX. The information of the corresponding sheet and new implemented control features will give the designer powerful assistance during the layout process.

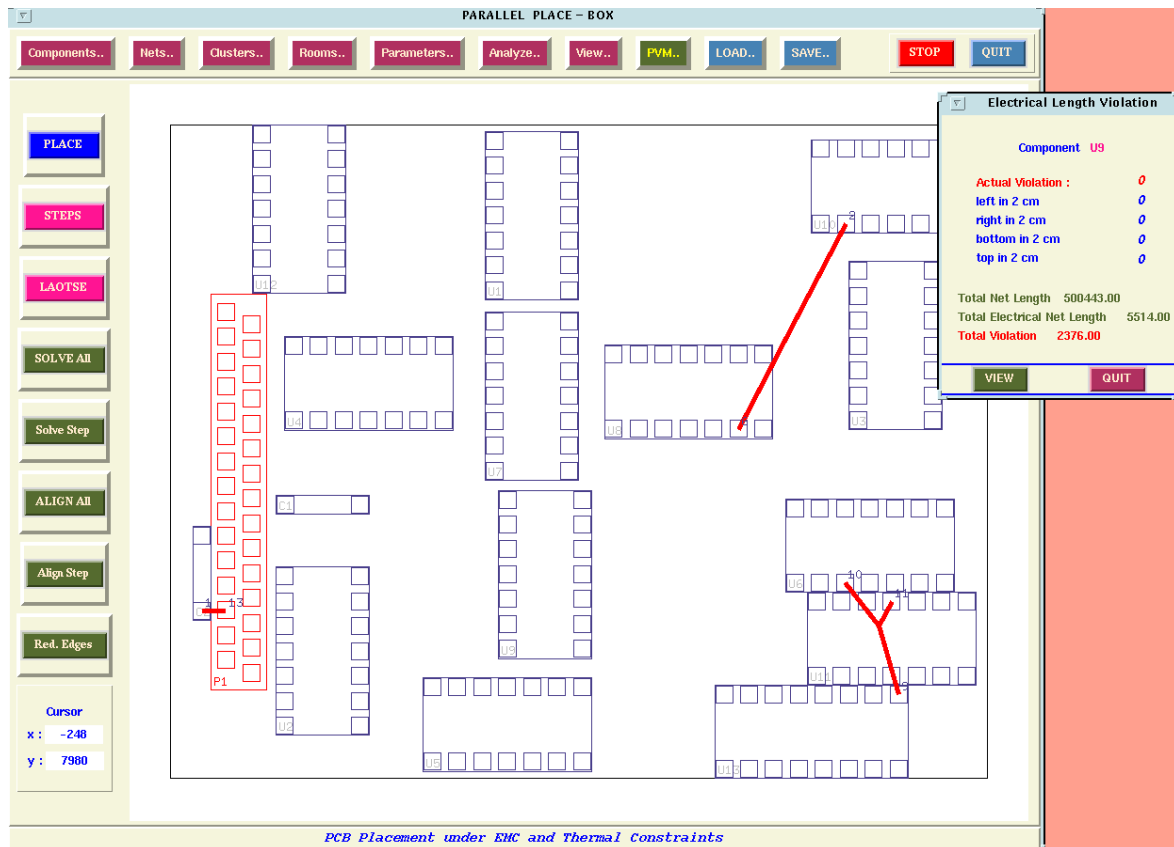


Figure 5: Control sheet of electrical length violations

3.3.3 Integrating PLACE-BOX into THEDA

One of the main tasks of the DAPPER project was the integration of PLACE-BOX into PCB design system THEDA. The integration was a strong prerequisite for evaluation and for the usage of the tool in the end-user design departments. For the integration, the input of the placement problem has to be extracted from the THEDA-database. This database contains very detailed geometrical information about the layout. The crucial task of realising an interface was to find an appropriate level of abstraction for these details such that the information provided are detailed enough to avoid violations of clearance rules and to be able to determine dense placement using tiny free spaces and on the other hand not to slow down the algorithms by considering unnecessary details. THEDA was extended to supply dialogue windows for the placement parameters and to select placement methods. These parameters have to be passed to PLACE-BOX as well. After the computation of PLACE-BOX has finished, the resulting component locations are transferred into the THEDA database and the result of the placement is displayed by the graphical user interface of THEDA.

The next two figures show the integration of PLACE-BOX into THEDA. Figure 6 shows the new Autoplacement parameter sheet of THEDA. As the control sheet for the Autorouter in THEDA, the control of the Autoplacement is organised in passes. In a pass one method can be specified. For the execution the method-dependent parameters, the set of components, pass-specific placement rules and a processing area to which the application of the method is restricted can be selected. The passes are stored in the persistent database and can be selected in any order for execution.

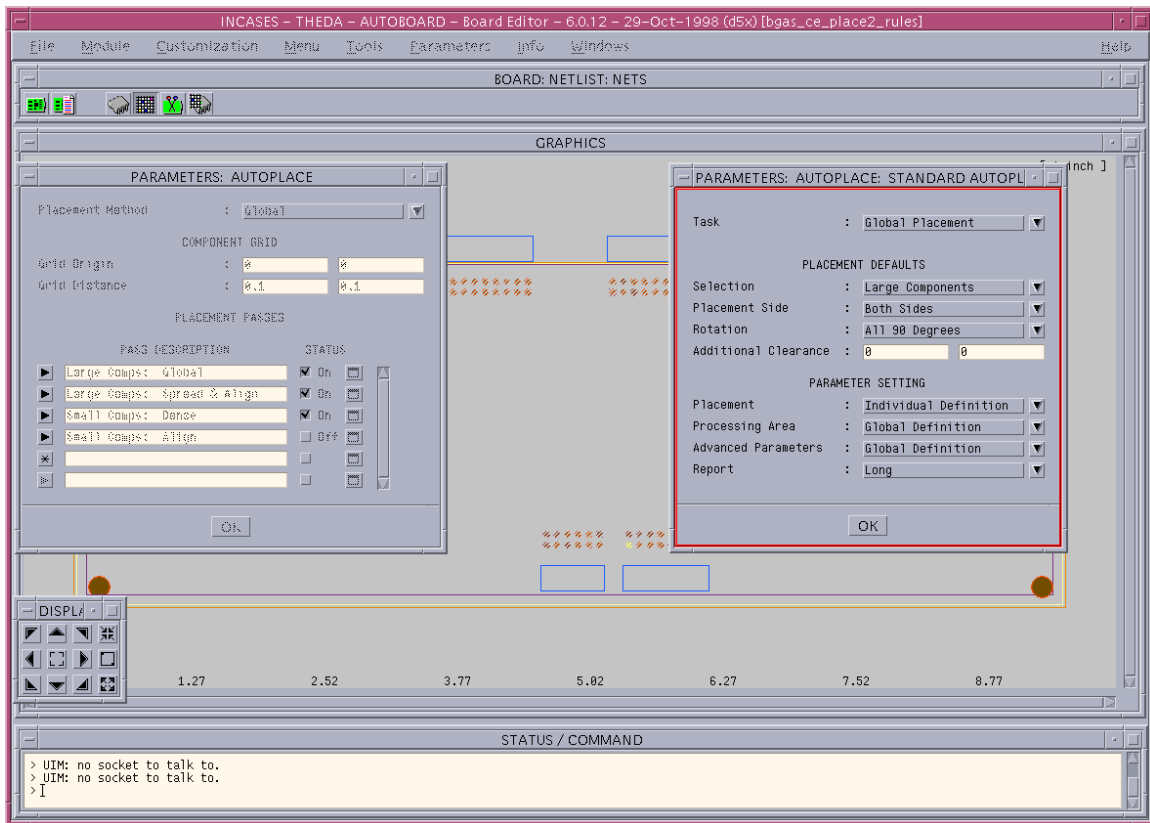


Figure 6: THEDA Autoplacement parameter sheet

Figure 7 shows a placement result computed by PLACE-BOX methods in THEDA.

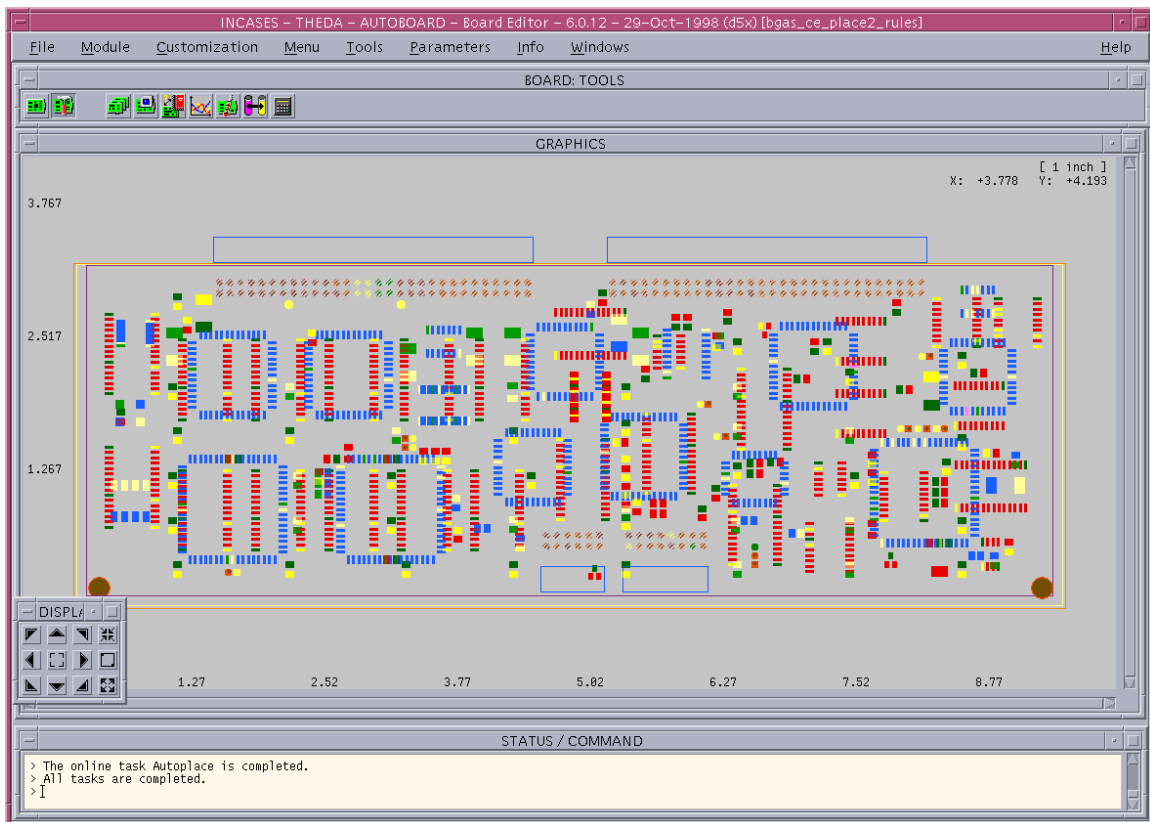


Figure 7: THEDA Placement

Integration into design systems like THEDA is a pre-requisite to sell the placement tool to the users.

3.3.4 Placement of Decoupling Capacitors

Caused by the technological progress in electronic design we were faced with several strong demands by the end-users for new placement methods and features. One of these demands was to solve the placement of decoupling capacitors efficiently. A good placement of the decoupling capacitors is necessary to ensure the functionality of the circuit. Up to now, the end-users place decoupling capacitors sequentially in a time consuming interactive way.

Now, a sophisticated method is integrated in placement tool PLACE-BOX. The method takes different design rules into account which were defined by the end-users. The components are placed by this method under consideration of all placement constraints. The special strategy for placing decoupling capacitors nearby the power/ground pins of ICs needs to know which ICs use which capacitors. For this, the user defines component clusters of all ICs that share the same decoupling capacitors.

Figure 8 shows a placement result delivered by this dedicated method.

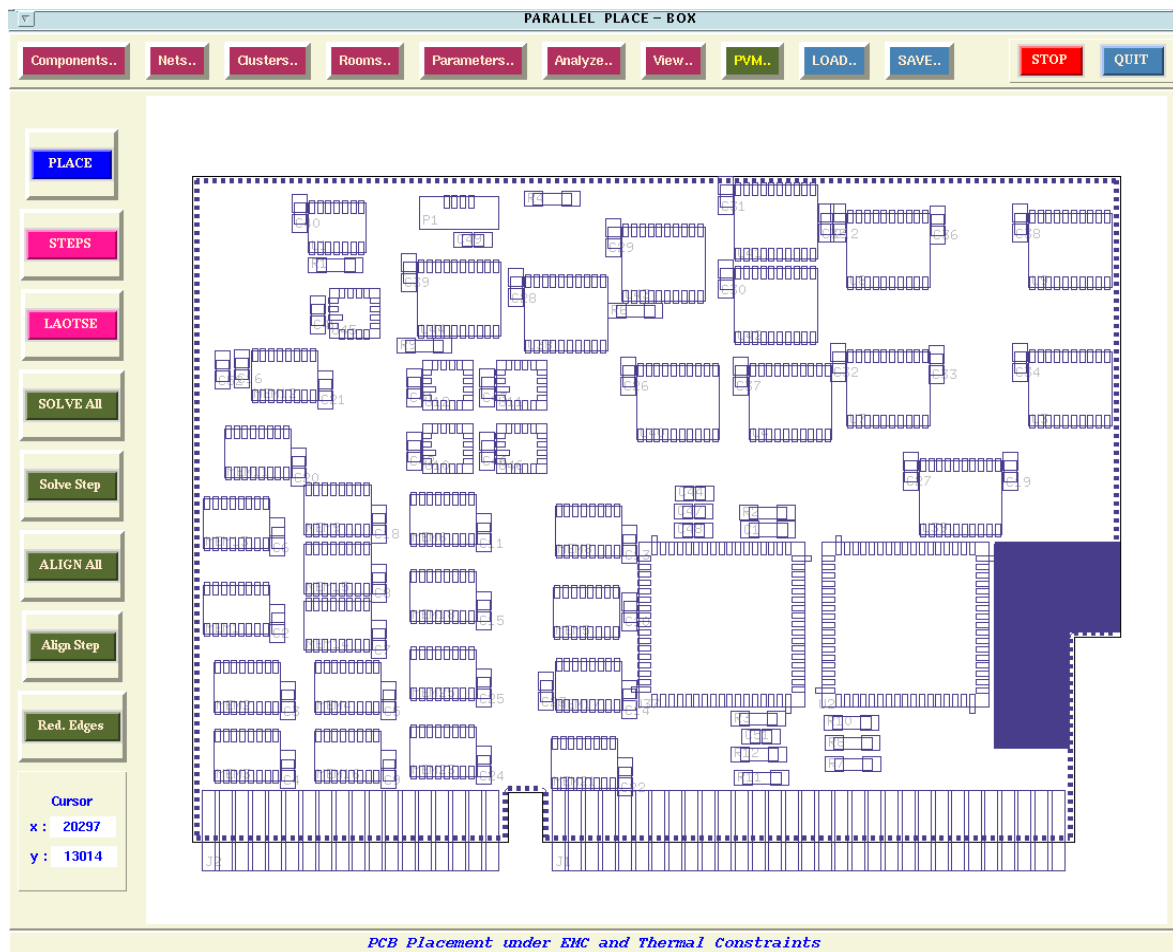


Figure 8: Placement of decoupling capacitors

This new method assists the layout designer in different ways to reduce the overall design time. First, to ensure the board functionality the dedicated placement strategy is flexible enough to place the capacitors nearby the power or ground pins of ICs as needed. Secondly, the time-consuming interactive manual placement of such capacitors can be substituted by this fast method. Sometimes the designer has to rotate an already placed IC with its capacitors. With this powerful method the designer can compute the necessary modification very fast.

3.3.5 Business Benefits

Placement of high density boards is one of the most crucial tasks in PCB design. As the European electronics industry is specifically strong in the area of system design (and systems are assembled by PCBs), placement tools are very important for the European industry, to keep the competitive edge.

During placement various constraints like thermal, EMC and manufacturability have to be considered. This results in such a complex task, that no automatic PCB placement tools are available respectively widely used in the industry. Therefore placement is done interactively and it can easily require several weeks to place dense high speed boards. The sequential place box developed by WIDIS provides an automatic PCB placement methodology, that is able to resolve most placement problems in about one hour. This is already a mayor step forward compared with interactive manual placement.

Unfortunately, this time is still too much to allow a more interactive usage of this autoplacement tool. But interactivity is required, if different placement options have to be worked out in order to find an optimal solution.

With the new parallel PLACE-BOX developed in the DAPPER project, the placement time could be reduced significantly by using distributed computing on a cluster of workstations. Now placement is possible in about ten minutes and the autoplacement technology has achieved a performance that is acceptable by the industry.

Additionally it has to be mentioned, this speed up has been achieved by exploiting available hardware clusters. Therefore no additional invest is required which makes the project results very attractive for small and medium size industry.

By integrating the new parallel placement technology into a professional design system (THEDA), it has been shown, that this technology can be used in commercial products.

3.4 *Dissemination*

This chapter addressed the dissemination and awareness creation actions that have been performed during the project.

3.4.1 *Target Audience*

With the following performed activities the project partners tried to introduce the envisaged placement tool with its new features to the PCB design community world-wide.

The target audience of the DAPPER project consists of

- the design departments of the end-user companies
- the world-wide customers of INCASES
- and EMC and PCB design experts world-wide.

3.4.2 *List of External Events*

- In September 1997 the annual INCASES User Group Conference took place in Paderborn. A lecture 'An advanced tool for placement under thermal and EMC requirements' was given by WIDIS and the University of Paderborn to inform the INCASES customers about the envisaged tool and the project objectives.
- Two EMC courses were organised and carried out by WIDIS in Munich (December 1997). During these events the placement tool with its ability of taking EMC constraints into account was introduced to about 40 EMC experts from Siemens.
- A software demonstration was given during a meeting of the Berlin FED group (January 1998). About 30 PCB experts visited this meeting. These experts were mainly coming from SMEs.
- In May 98 the University of Paderborn and INCASES demonstrated the placement tool to customers of INCASES (Matra BAe, Marconi, British Gas). The customers confirmed the strong need for an EMC driven placement tool with the envisaged features.
- At 1998-07-22 a press conference about the new placement tool took place in Munich. INCASES informed journalists from 6 journals (Elektronik, F&M, Elektronik Informationen, Elektronik Industrie, Markt&Technik, Systeme).
- To inform the PCB design community world-wide an article about the aims of the DAPPER project was published in the INCASES newsletter INSIGHT (issue 2/98, June). Figure 9 shows a snapshot of this article.

INCASES is Partner in ESPRIT Project 'DAPPER'

by/von Peter Wunderlich
R&D Manager, THEDA

INCASES, WIDIS, BOSCH and the University of Paderborn are collaborating in a joint project called 'DAPPER' (Distributed and Parallel Application of PCB Placement Methods for EMC Driven Design) which began on June 1 last year.

The project investigates new placement methods based on parallel and distributed processing on a cluster of workstations to reduce the computation time for highly complex placement tasks significantly. The DAPPER project is an activity in the frame of the ESPRIT work program domain HPCN (High Performance Computing and Networking). The European Commission promotes the use of HPCN at large to strengthen the European Industry, especially small and medium size enterprises.

INCASES is the industrial partner expected to commercialise the results of the project, and BOSCH is the industrial evaluator partner. The results of the DAPPER project are being commercialised through inclusion of the algorithms in INCASES' CE-PLACER and through updates to this product throughout the period of the project, and will provide enhancements to both the uni-processor environment and in distributed processor environments. ■

INCASES ist Partner beim ESPRIT-Projekt 'DAPPER'

Gemeinsam mit den Firmen WIDIS, BOSCH und der Universität von Paderborn arbeitet INCASES an einem Projekt im Rahmen des europäischen ESPRIT-Programms, genannt 'DAPPER' (Distributed and Parallel Application of PCB Placement Methods for EMC Driven Design), das am 1. Juni des vergangenen Jahres gestartet wurde. Im Rahmen dieses Projektes sollen neue Platzierungsmethoden erarbeitet werden, die parallel in einem Cluster von Workstations verteilt bearbeitet werden können, um die Rechner- (Computing) Zeit für hochkomplexe Platzierungsaufgaben deutlich zu reduzieren.

Das DAPPER-Projekt gehört zum ESPRIT-Arbeitsprogramm HPCN (High Performance Computing and Networking). Das Projekt wurde aufgelegt, um die europäische Industrie zu stärken und zwar ganz besonders kleine und mittlere Unternehmen.

INCASES hat den Part übernommen, die Ergebnisse des Projektes zu kommerzialisieren, während Bosch diese praktisch evaluieren wird. U.a. werden die Ergebnisse des DAPPER-Projekts dadurch kommerzialisiert, daß die Algorithmen im INCASES CE-PLACER integriert werden und während des Projektzeitraums ständig upgedated werden. Es sollen Verbesserungen sowohl für Ein-Processor-, als auch verteilte Prozessor-Umgebungen erzielt werden. ■

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INCASES INSIGHT Issue/Ausgabe 2/98

Figure 9: Snapshot of the INSIGHT article

- An EMC course was organised and carried out by WIDIS in Salzburg (1998-06-26). During this event the placement tool with its ability of taking EMC constraints into account was introduced to 10 EMC experts.
- In September 98 WIDIS gave an EMC lecture at the CIM-Team user meeting in Ulm. During this event the placement was introduced to more than 100 customers.
- INCASES gave a lecture and software demonstration during the German User Group meeting in Bayreuth to more than 40 customers.
- WIDIS presented the parallel PLACE-BOX in the frame of the FED conference in September 98. This annual conference was visited by more than of 200 PCB Design experts and electronic engineers from Germany and from abroad.
- In order to transfer the project results to the PCB design groups of INCASES and BOSCH, the end-users gave presentations in their companies on their experiences.
- INCASES continuously informed their world-wide customers about the new placement tool. Today more than 150 companies world-wide (mainly SMEs altogether with several

1000 licenses) are using THEDA. Each of them is a potential user of the new placement tool.

3.4.3 Dissemination Material

Flyer

In March and November 1998 DAPPER information flyers were designed and printed. Both flyers have been printed in order to facilitate dissemination activities. These flyers, printed at WIDIS, give a global overview of the DAPPER project, whereas the second one tends to highlight the project outcome and the industrial benefits. Figure 10 shows a snapshot of one side of this flyer.

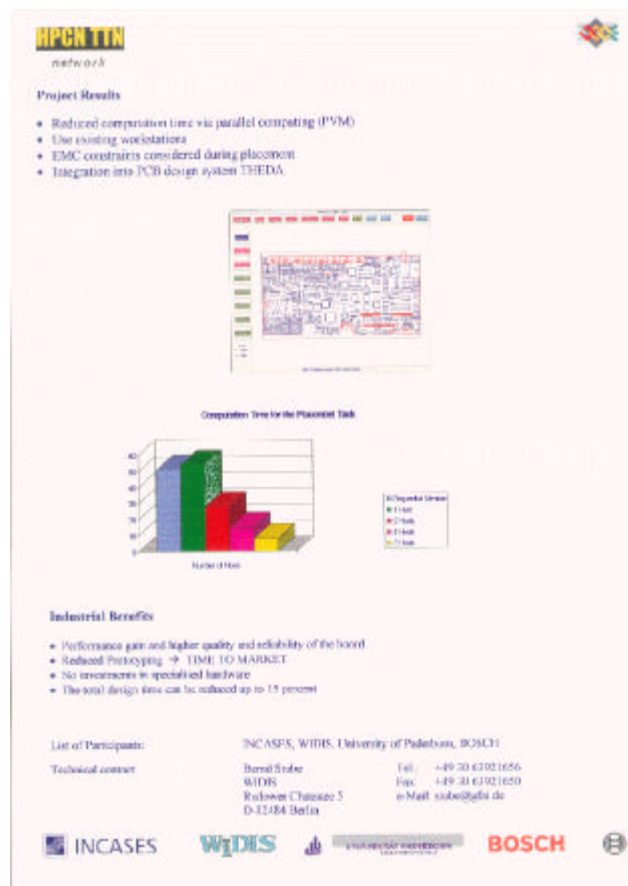


Figure 10: Snapshot of the DAPPER information flyer

Web Pages

A WWW presentation of the DAPPER project, the partners, the objectives and expected results was delivered in March 1998. The URL is : www.widis.de/projects/dapper.htm Based on the project results the project presentation was updated and extended in December 1998. Figure 11 shows a snapshot of the first page of the WWW presentation.

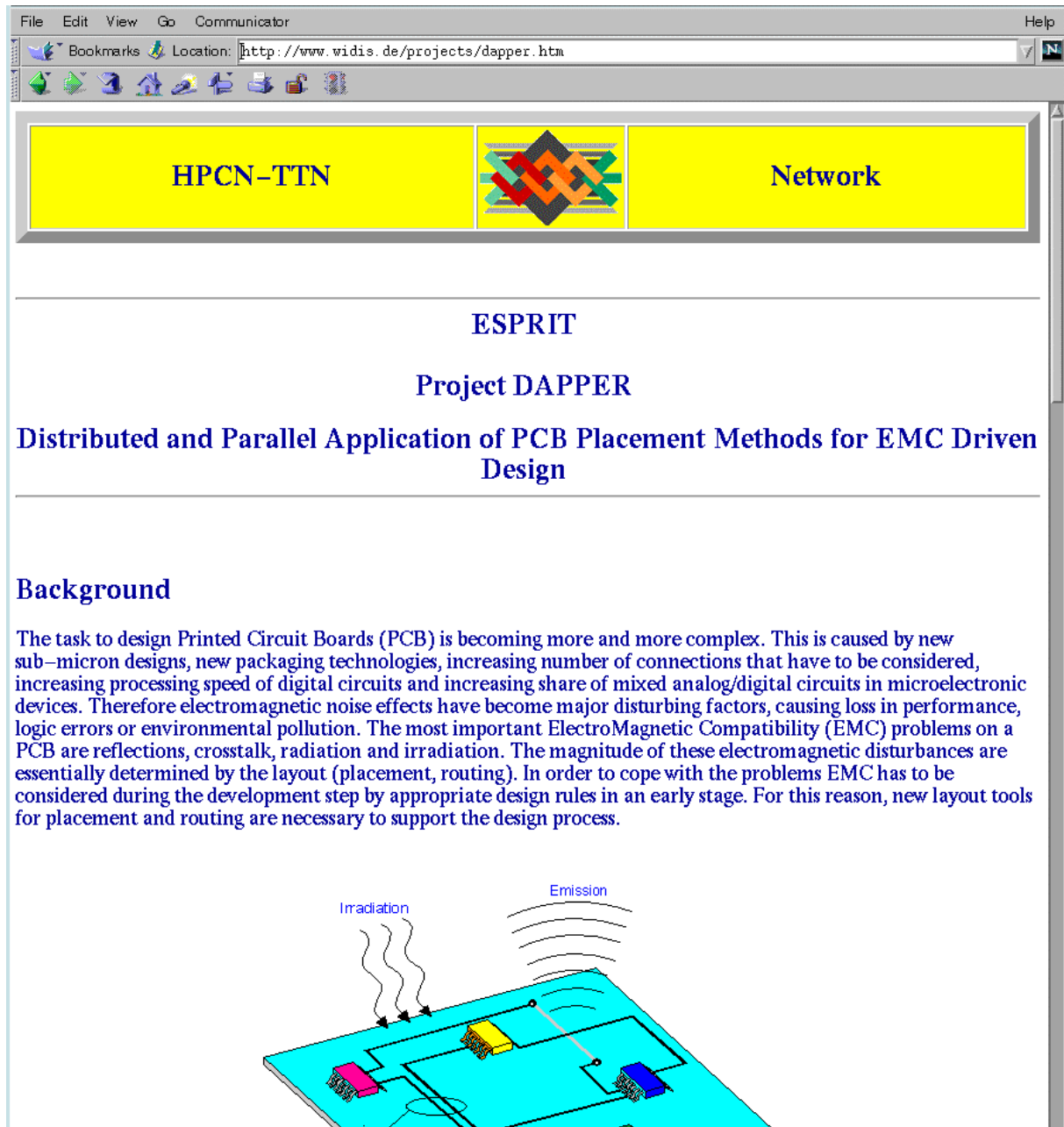


Figure 11: Snapshot of the project WWW presentation

3.4.4 Publications

☒ Paper for Electronic Design '97

WIDIS and the University of Paderborn gave a lecture 'Ein neues Tool zum EMV-gerechten Platzieren von Bauelementen' at the FED (Fachverband 'Elektronik Design') conference Electronic Design '97 (Celle (Germany), September 1997).

Ein neues Tool zum EMV-gerechten Plazieren von Bauelementen

von

Bernd Stube¹ und Henrik Schmidt²

¹ WIDIS GmbH Berlin

² C-Lab Paderborn

Zusammenfassung:

Die Platzierung von Bauelementen auf einer Leiterplatte unter Berücksichtigung von EMV-, thermischen-, geometrischen und technologischen Restriktionen ist eine hoch komplexe Entwurfsaufgabe, deren Bedeutung immer mehr zunimmt. Insbesondere EMV und thermische Anforderungen erfordern die Anwendung von global optimierenden Verfahren, damit die gleichzeitige Berücksichtigung aller Netze realisiert werden kann. In dem Beitrag wird ein neues Platzierungstool PLACE-BOX vorgestellt, das diese Restriktionen bei der Platzierung berücksichtigt. Nach Ausführungen über die Problematik wird in dem Beitrag das Konzept des Tools vorgestellt. Ausgewählte Verfahren werden skizziert und es wird die Leistungsfähigkeit des Tools anhand von Beispielen demonstriert.

Summary:

Placement of components on a PCB under EMC, thermal, geometrical and technological constraints is a highly complex design task which gets more and more important. Especially EMC and thermal constraints require the application of global optimising methods in order to simultaneously consider all nets. In this paper the new placement tool PLACE-BOX is presented with its concept and selected methods.

☒ Paper for PVM-MPI User's Group Meeting '97

The University of Paderborn gave a lecture 'Parallel Branch and Bound Algorithms for Integer and Mixed Integer Linear Programming Problems under PVM' at the Fourth European PVM-MPI User's Group Meeting (Krakow (Poland), November 1997).

Parallel Branch and Bound Algorithms for Integer and Mixed Integer Linear Programming Problems under PVM

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² C-LAB/Analog System Engineering · University of Paderborn · Paderborn · Germany

Abstract. In this paper we consider efficient parallel Branch and Bound (B&B) algorithms for Integer Linear Programming (ILP) and Mixed ILP (MILP) Problems in a MIMD distributed memory environment. The algorithms are scalable and run on a cluster of workstations under PVM. To achieve efficient parallel implementation and to speedup the computations in our approach, **firstly**, we apply various preprocessing techniques in order to reduce the problem size prior to optimization, and **secondly**, we apply B&B algorithms with dynamic distribution of tasks among the processors.

The efficiency of the algorithms has been investigated and the test results on examples from MIPLIB library and real life problems arising in Printed Circuit Boards and Multi Chip Modules layout are presented.

3.5 Conclusions

Demonstration project DAPPER has successfully demonstrated the economical benefit of the application of HPCN technologies in the field of PCB layout design. Both main tasks of the project the parallelisation of placement tool PLACE-BOX by using distributed processing and the integration into design system THEDA are realised as proposed. A very important fact for the success of the project was the good constitution of the project team (1 technology provider, 1 HPCN expert, 2 end-users). So, it was continuously guaranteed that the project was end-user driven and the project outcome would match the market needs. Since the placement tool is working on a cluster of workstations there is the opportunity to use the project outcome in SMEs of this industrial sector. This aspect fulfilled a main objective of the ESPRIT frame. Based on the gathered HPCN experiences the end-users will evaluate more processes in their companies for a successful application of parallelisation and distribution techniques. The successful co-operation between the project partners and the co-ordinating organisation TTN CAPRICE was a good base for the project success.

3.5.1 Technical Goals

The parallel placement tool is realised as proposed. It was successfully applied to different demonstration examples and during the evaluation phase to latest designs of the end-users. These boards were manually placed and routed in the companies. The design processes were very time consuming due to the extreme board complexity and many restrictions. Based on the gathered results it was shown that the parallel tool reduced the computation time for placement significantly. Depending on the design task the new placement tool is able to reduce the overall

design time up to 15 percent. Based on the technological progress the project was faced with demands by the end-users for new placement features. Therefore, several new algorithms are developed and integrated in PLACE-BOX, e.g., a new sophisticated method for placing decoupling capacitors. The placement tool is successfully integrated into PCB design system THEDA. This integration is a prerequisite for evaluation and for usage in the design departments of the end-users.

3.5.2 Business Benefits

The present project has clearly demonstrated that substantial savings can occur by using parallel and distributed processing. The results show that the following business benefits can be achieved by using the new placement tool:

- **Decreased time to market**

By taking the routing step into account and depending on the design task the total design time can be reduced up to 15 percent by using the tool.

- **Reduced prototyping**

By taking EMC requirements during placement into account the tool can reduce the number of design cycles and can avoid time consuming and expensive redesigns.

- **Higher product quality**

The consideration of EMC constraints in an early stage of the design process ensures a higher quality of the products.

- **Improved design work**

Based on distributed processing the tool with its time behaviour is well suited for interactive design work.

- **Usage in SMEs**

Since the tool is working on a cluster of workstations no investment in specialised and expensive hardware is necessary. Therefore, the placement tool can be easily used in SMEs.

- **Increased competitiveness**

The project outcome increases the competitiveness of the end-users and will be delivered to market.

3.5.3 Exploitation

The placement tool will be introduced in the design departments of the end-users BOSCH and INCASES. Currently, they do not use automatic layout design tools. In order to get a significantly reduction of costs and development time of products the tool introduction requires a change of their applied design methodology. The necessary changes including new company specific defined design steps will be prepared. After successful introduction BOSCH will check the tool transfer to other design departments of the company.

Since there is no commercial tool on market which used global optimising methods and can take such complex design requirements into account, the tool is expected to be successful on the market. INCASES has shown its ability to commercialise and support EDA software tools since the company inception in November 1994. Since that time it has rapidly extended their initial 2 product families and introduced a third product family to the market. The project outcome will be tested, productized and marketed to the same high standards as all existing INCASES products. The tool will be sold as an add-on option to the THEDA product line. Today more than 150 companies world-wide (mainly SMEs altogether with several 1000 licenses) are using THEDA. Each of them is a potential user of the new placement tool. INCASES will use the project outcome to increase the level of differentiation between itself and its competitors.

3.6 Contact Details

The following table summarises the contact persons of the DAPPER project:

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Web Site

Information about the project can be found on the following URL:

www.widis.de/projects/dapper.htm

Project Duration

Start: June 1997
End: December 1998

Budget

The global cost of the project was 306.648 ECU, the EC has funded 196.491 ECU. The remaining resources have been funded by the project partners.