

DAPPER



HPCN TTN Network

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DAPPER speeds up the development of printed circuit boards

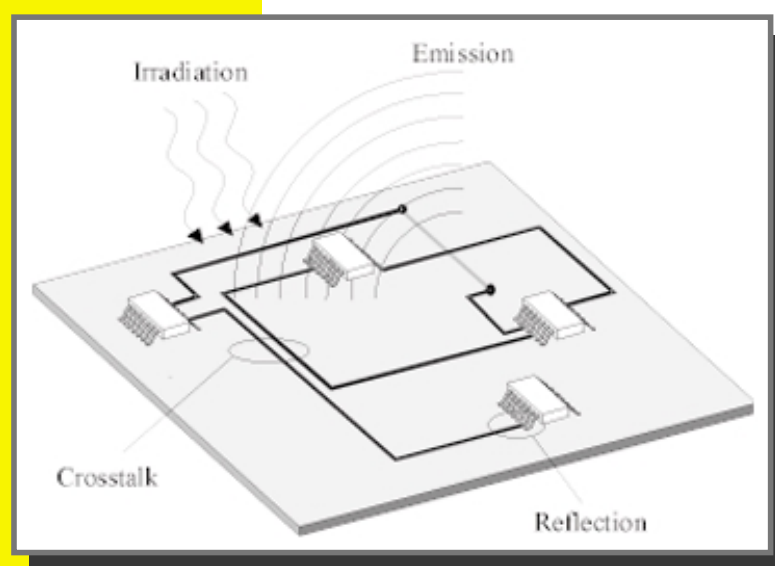
In designing printed circuit boards (PCB) electromagnetic compatibility (EMC) must be assured. Even in existing designs, technological innovations in individual PCB components can cause new incompatibilities, resulting in reflections, crosstalk, radiation and irradiation.

New layout tools can optimize EMC by applying rules early on in PCB layout and design. One such tool is PLACE-BOX, a PCB layout program that uses global optimising methods to determine the best placement of components. But until now, its sequential processing made it too time-intensive to be truly competitive.

The solution is parallelisation. DAPPER - **D**istributed and **P**arallel **A**pplication of **P**CB **P**lacement **M**ethods for **E**MC **D**riven **D**esign - is an EU-funded project that uses High Performance Computing and Networking (HPCN) to parallelise PLACE-BOX processing. This makes PLACE-BOX a commercially viable tool that even medium-sized enterprises can easily implement. Since the tool runs on a cluster of workstations, no investment in specialised and expensive hardware is necessary.

DAPPER's benefits:

- Total design time reduced by up to 15%
- Reduced prototyping
- Higher product quality
- Higher design efficiency through interactive use of PLACE-BOX



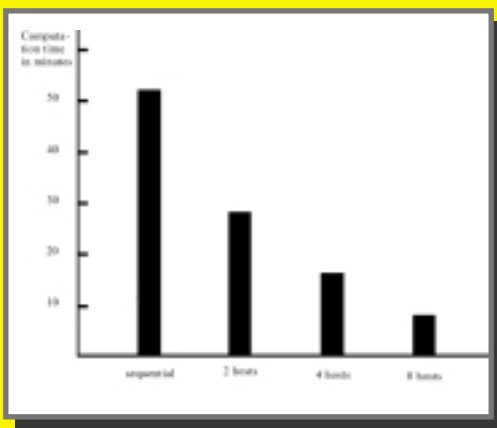
Electromagnetic interference sources

Right place, right time

DAPPER parallelises the sequential placement tool PLACE-BOX and integrates it into the PCB design system THEDA. The resulting system cuts development time so that the same high-quality PCBs can be produced faster.



DAPPER distributing PLACE-BOX tasks among several workstations



10 minutes computing time with DAPPER versus 51 minutes without

Like most engineering tasks, PCB design involves trade-offs. Certain requirements are contradictory, e.g. thermal considerations call for wide spacing of components while electrical efficiency requires close grouping. These situations require decisions that only an experienced PCB developer can make.

Parallelised PLACE-BOX generates a rule-based basic layout within just a few minutes. This rough draft already meets the fundamental design requirements. The developer can then concentrate on optimising the layout and resolving any trade-off issues. The short run times made possible by DAPPER thus allow fast interactive work between human developer and computer, for efficient use of time and skills.

In actual use, sequential PLACE-BOX took about 51 minutes for the 8 cycles needed to compute the placement result for a typical board. The parallel DAPPER version needed only 10 minutes on a cluster of 4 SUN workstations.

High Performance Computing and Networking Programme

The HPCN Programme is an EU initiative that makes high-performance computing available to small and medium-sized enterprises. This is supported by a pan-European network of 21 Technology Transfer Nodes (TTNs). Each TTN acts as a resource centre, providing access to the combined know-how of the entire HPCN TTN Network and contacts to firms and experts engaged in other HPCN projects. Currently some 150 projects are underway.



For more information see <http://widis.de/projects/dapper.htm> or contact a DAPPER project partner:

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